

**Table 7-7** (continued)  
IOU signal descriptions

Pin	Signal	Description
25	PRAS'	Row-address strobe (phase 0)
26	$\phi 0$	Master clock phase 0
27	Q3	Intermediate timing signal
28	+5V	Power
29	A6	Address bit 6 from 65C02
30	C0xx	I/O address enable
31	AKD	Any-key-down signal
32	KSTRB	Keyboard strobe signal
33,34	VIDD7,VIDD6	Video display data bits
35,36	RA9',RA10'	Video display control bits
37	CLRGAT'	Color-burst gate (enable)
38	WNDW'	Display blanking signal
39	SYNC'	Display synchronization signal
40	H0	Display horizontal timing signal (low bit of character counter)

## The PAL device

A Programmed Array Logic device, type PAL 16R8, generates several timing and control signals in the Apple IIe. These signals are listed in Table 7-8. The PAL pinouts are given in Figure 7-4.

**Table 7-8**  
PAL signal descriptions

Pin	Signal	Description
1	14M	14.31818 MHz master timing signal
2	7M	7.15909 MHz timing signal
3	3.58M	3.579545 MHz timing signal
4	H0	Horizontal video timing signal
5	VID7	Video data bit 7
6	SEGB	Video timing signal
7	GR	Video display graphics-mode enable
8	RAMEN'	RAM enable (CAS enable)
9	80VID'	Enable 80-column display mode

14M	1	20	+5V
7M	2	19	PRAS'
3.58M	3	18	(n.c.)
H0	4	17	PCAS'
VID7	5	16	Q3
SEGB	6	15	$\phi 0$
GR	7	14	$\phi 1$
RAMEN'	8	13	VID7M
80VID'	9	12	LDPS'
GND	10	11	ENTMG

**Figure 7-4**  
PAL pinouts